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## Patent Abstracts of Japan

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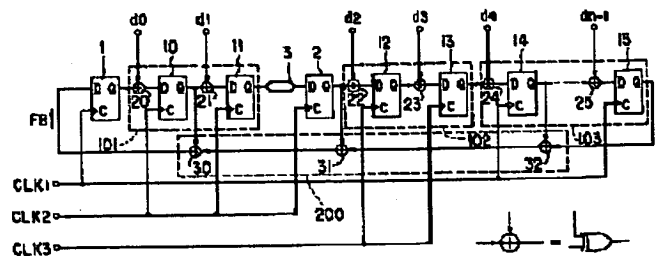
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APPLICANT : TOSHIBA CORP;

INVENTOR : NOZUYAMA YASUYUKI;

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TITLE : LINEAR FEEDBACK SHIFT REGISTER  
AND SEMICONDUCTOR INTEGRATED  
CIRCUIT DEVICE



ABSTRACT : PURPOSE: To provide a linear feedback shift register for satisfying the conditions of pseudo random number generation or linear feedback while being provided with F/Fs operated by mutually different clocks and a semiconductor integrated circuit device provided with the linear feedback shift register.

CONSTITUTION: The plural sets 101, 102 and 103 of the F/Fs operated in synchronism with the mutually different clocks CLK1, CLK2 and CLK3 are provided and the F/F 1 for satisfying the conditions of the pseudo random number generation or the linear feedback or mutually serially connected F/F 2 and a delay 3 are inserted mutually among the sets 101, 102 and 103 of the F/Fs. By this constitution, even when the sets 101, 102 and 103 of the F/Fs are operated in synchronism with the mutually different clocks CLK1, CLK2 and CLK3, output from the desired set of the F/Fs is delayed and signals propagated to the sets 101, 102 and 103 of the F/Fs satisfy the conditions of the pseudo random number generation or the linear feedback by the delay.

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